In the Specification

Amend the specification as follows:

Amend the paragraph beginning at page 2 line 3 as follows:

More recent lithographic monitoring improvements have been in optical metrology which rely on human or machine-read visual measurement of targets which employ arrays of elements having line widths and spacing below the wavelength of the light used to make the measurements. Improvements in monitoring bias in lithographic and etch processes used in microelectronics manufacturing have been disclosed in U.S. Patent Nos. 5,712,707; 5,731,877; 5,757,507; 5,805,290; 5,953,128; 5,965,309; 5,976,740; 6,004,706; 6,027,842; 6,128,089 and 6,130,750, the disclosures of which are hereby incorporated by reference. The ~~targets~~target and measurement methods of these patents rely on the increased sensitivity to process variation provided by image shortening. Some of these types of targets use image shortening effects to make the visual measurements of even though the individual array elements are not resolvable. Examples of such targets are disclosed in the aforementioned U.S. patents. Such targets permit visual monitoring of pattern features of arbitrary shape with dimensions on the order of less than 0.5 micron, and which is inexpensive to implement, fast in operation and simple to automate. These determine bias to enable in-line lithography/etch control using optical metrology, wherein SEM and/or AFM metrology is required only for calibration purposes.

Amend the paragraph beginning at page 3 line 14 as follows:

It is yet another object of the present invention to provide a method of ~~to~~ separating the effects of dose and focus in lithographic processing in a target or monitor which can be formed on a single lithographic layer on a wafer substrate.

Amend the paragraph beginning at page 4 line 17 as follows:

The edges of the array in the first mask portion are preferably substantially parallel to edges of the array in the second mask portion, and the elements in the first mask portion are preferably substantially perpendicular to the elements in the second mask portion. The pitch between elements of the arrays in the second mask sensitive portion is less than the resolution limit of the energy beam in the imaging system used to expose the mask in the lithographic processing. The second, dose sensitive mask portion may include a plurality of outer elements on each side of the central element, with the width of the outer elements decreasing with distance from the central element. The elements of the first and second mask portions may ~~comprises~~ comprise opaque elements on a substantially transparent mask substrate, or may comprise substantially transparent elements on an opaque mask substrate.

Amend the paragraph beginning at page 11 line 9 as follows:

An example of a lithography process using a mask made in accordance with the present invention is shown in Fig. 2. Radiation comprising energy beam 30 passes through a portion of mask 18 comprising a substrate layer 20 sufficiently transparent to the radiation on which are deposited opaque segments conforming to the target image to be projected.

Opaque segments 16 comprise ~~a the~~ the parallel array of elements and form a portion of the total target portion of the lithography mask. The beam 30 portion that passes through the mask 18 between opaque segments 16 is illustrated by beam 30a. Beam 30a is focused by lens system 24 onto the surface 32 of a semiconductor wafer having conventional resist materials sensitive to the radiation. Radiation blocked by mask portions 16 does not transfer to the resist layer on surface 32. Thus, a contrasting latent image of the parallel array elements 16 is formed on wafer resist surface 32 which conforms to the pattern of the opaque layer on the mask. The resist is then developed, and the resist pattern created by the latent image is used to etch a desired target or portion thereof on the wafer. The target of the present invention is employed to determine the quality of the lithographic formation of functional circuits elsewhere on the wafer.

Amend the paragraph beginning at page 12 line 12 as follows:

The second, primarily dose sensitive mask portion 14 comprises an array of elements which includes a central element having a length in the vertical direction and a width in the horizontal direction. On each side of central element 38 are a plurality of spaced, substantially parallel outer elements 40a, 40b, 42a, 42b, 44a, 44b, also having a length in the vertical direction and a width in the horizontal direction. The width of each of the outer elements is less than the width of the central element, and decreases with increasing distance of each outer element from the central element. As shown, on the right side of central element 38, the width of element 42a is less than the width of element 40a, and the width of element 44a is less than the width of element 42a. Likewise, ~~one~~ on the left of the central

element, the width of element 42b is less than the width of element 40b, and the width of element 44b is less than the width of element 42b. Other outer elements may be added as desired, however, the dose sensitive target is useful with even a single outer element spaced from and adjacent to a central element. The edges of outer elements 44a, 44b on each side of and farthest from central element 38 form opposing array edges. The sum of the width of each outer element and the spacing which separates the outer element from another element is the outer element pitch P_2. To ensure that the outer elements are not resolved, P_2 is kept constant with increasing distance of each outer element from the central element. Alternatively, the width of the elements 40, 42, 44 could be kept constant while P_2 decreases; however, this would be a more difficult pattern to fabricate.

Amend the paragraph beginning at page 20 line 4 as follows:

Accordingly, the present invention provides an electrically testable structure to solve relative dose, focus and etch problems which is easy and inexpensive to utilize and which utilizes little space on a wafer substrate. The electrically testable monitor of the present invention is particularly useful for automated systems and ~~do~~ does not require visual monitoring.